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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/288,263 | 04/08/1999 | HIROYUKI WAKI | NAK1-BG55 | 7236 |

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| EXAMINER | |
|---|---|
| LAFORGIA, CHRISTIAN A | |
| ART UNIT | PAPER NUMBER |
| 2157 | |

DATE MAILED: 10/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/288,263 | WAKI ET AL. | |
| | Examiner | Art Unit | |
| | Christian La Forgia | 2157 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *9/23/02* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7,19-24,29-31,36,37 and 39-51* is/are pending in the application.

4a) Of the above claim(s) *1-7,19-24,36 and 37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-31, 39-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-7, 19-24, 36, 37* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *PTO-1533* .

## DETAILED ACTION

1. Group I, claims 1 through 6, are non-elected.

2. Group II, claim 7, is non-elected.

3. Group III, claims 8 through 18, 33, 34, and 35, are non-elected.

4. Group IV, claims 19 through 24, are non-elected.

5. Group V, claims 25 through 28, 32 and 38, are non-elected.

6. The amendment filed on 23 September 2002, is noted and made of record.

7. Claims 29 through 31 and 39 through 51 are presented for examination.

8. Claims 8 through 18, 25-28, 32-35, and 38 have been canceled without prejudice.

9. Claims 1 through 7, 19 through 24, 36, and 37 have been withdrawn.

10. This application contains claims 1 through 7, 19 through 24, 36 and 27 are drawn to an invention nonelected with traverse in Paper No. 7. A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

### *Drawings*

11. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

***Claim Rejections - 35 USC § 102***

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

13. Claims 29, 30, and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,021,469 to Tremblay et al., (hereinafter Tremblay).

14. As per claim 29, Tremblay teaches a storage method used by instruction storing means that stores a virtual machine instruction sequence to be executed by a virtual machine, having a stack architecture, under control of a real machine (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57),

15. the storage method being characterized by storing each virtual machine instruction in the virtual machine instruction sequence associated with different succeeding instruction information, the succeeding instruction information for a given virtual machine instruction indicating a change in a storage state of data in a stack due to execution of a virtual machine instruction executed after the given virtual machine instruction (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57).

16. Regarding claim 30, Tremblay teaches a storage method used by instruction storing means that stores a virtual machine instruction sequence to be executed by a virtual machine

under control of a real machine (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57),

17. wherein the storage method results in:

18. the instruction storing means being a plurality of instruction blocks that constitute the virtual machine instruction sequence, the instruction blocks corresponding to basic blocks (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57);

19. the instruction blocks including:

an identifier area for storing an identifier that specifies a start position of the instruction block in the instruction storing means (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57);

a non-branch instruction area for storing non-branch instructions belonging to a corresponding basic block (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57);

a branch instruction area for storing at least one branch instruction belonging to the corresponding basic block (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57); and

20. each branch instruction stored in the branch instruction area designating a branch destination using an identifier stored in one of the identifier areas (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57).

21. Regarding claim 45, Tremblay teaches a computer-readable recording medium for recording a program that enables a computer to carry out the storage method (Figures 1 & 3; column 5, line 36 to column 6, line 54; column 7, lines 51-63).

22. Claims 39 through 41, and 46 through 48 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,151,618 to Wahbe et al., (hereinafter Wahbe).

23. Regarding claim 39, Wahbe teaches a storage method used by instruction storing means that stores a virtual machine instruction sequence to be executed by a virtual machine under control of a real machine,

24. wherein the storage method results in:

25. the instruction storing means being a plurality of instruction blocks that constitute the virtual machine instruction sequence, the instruction blocks corresponding to basic blocks (Figures 4, 6, & 7; column 11, line 58 to column 12, line 13);

26. the instruction blocks each including:

an identifier area for storing an identifier that specifies a start position of the instruction block in the instruction storing means (Figures 4, 6, & 7; column 12, lines 14-30);

a non-branch instruction area for storing non-branch instructions belonging to the corresponding basic block (Figures 4, 6, & 7; column 11, line 58 to column 12, line 13); and,

a branch instruction area for storing at least one branch instruction belonging to the corresponding basic block (Figures 4, 6, & 7; column 11, line 58 to column 12, line 13).

27. As per claim 40, Wahbe teaches wherein the identifier of the instruction block is address related information in the virtual machine instruction sequence (Figures 4, 6, & 7; column 12, lines 14-30).

28. As per claim 41, Wahbe teaches wherein the address related information is one of absolute address, relative address, and offset address (Figures 4, 6, & 7; column 12, lines 14-30).

29. As per claims 46 through 48, Wahbe teaches a computer-readable recording medium for recording a program that enables a computer to carry out the storage method (Figures 1 through 3; column 5, line 20 to column 7, line 12).

***Claim Rejections - 35 USC § 103***

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay in view of United States Patent No. 4,177,514 to Rupp.

32. As per claim 31, Tremblay teaches a computer-readable recording medium that stores a program to have a computer function as a virtual machine with a stack architecture (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57),

33. wherein the virtual machine comprises:

34. instruction storing means for storing a virtual machine instruction sequence and a plurality of sets of succeeding instruction information, wherein each virtual machine instruction in the virtual machine instruction sequence is associated with a set of succeeding instruction information that indicates a change in a storage state of the data in the stack means due to an execution of a virtual machine instruction executed after the associated virtual machine instruction (Figure 1; column 7, lines 30-57);

35. read means for reading a virtual machine instruction and an associated set of succeeding instruction information from the instruction storing means (Figure 1; column 7, lines 30-57); and,

36. decoding executing means for specifying and executing operations corresponding to a combination of the read virtual machine instruction and the read set of succeeding instruction information (Figure 1; column 5, line 36 to column 6, line 28; column 7, lines 30-57).

37. Tremblay does not teach a stack means for temporarily storing data in a last-in first-out format.

38. Rupp teaches a stack means for temporarily storing data in a last-in first-out format (column 53, line 63 to column 54, line 7). Therefore, it would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the stack management

means of Rupp with the system of Tremblay, because it would enable a quick and efficient way to manage the stack.

39. Claims 42 through 44 and 49 through 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wahbe in view of Tremblay.

40. As per 42, Wahbe does not teach wherein whether each virtual machine instruction is positioned at a start position of the basic block is indicated by an address in the virtual machine instruction sequence to which the virtual machine instruction is allocated;

41. a virtual machine instruction at the start position of the basic block being allocated to a specific address in the virtual machine instruction sequence, and

42. a virtual machine instruction at other than the start position of the basic block being allocated to an address other than the specific address.

43. Tremblay teaches wherein whether each virtual machine instruction is positioned at a start position of the basic block is indicated by an address in the virtual machine instruction sequence to which the virtual machine instruction is allocated (Figures 4A & 4B; column 19, line 1 to column 21, line 5);

44. a virtual machine instruction at the start position of the basic block being allocated to a specific address in the virtual machine instruction sequence (Figures 4A & 4B; column 19, line 1 to column 21, line 5), and

45. a virtual machine instruction at other than the start position of the basic block being allocated to an address other than the specific address (Figures 4A & 4B; column 19, line 1 to column 21, line 5). It would have been obvious to one with ordinary skill in the art at the time

the invention was made to include the addressing of Tremblay with the system of Wahbe, because it would create a quicker and more efficient method to access the next sequence of data.

46. As per claim 43, Wahbe teaches an identifying unit for storing identification information which indicates if the virtual machine instruction is positioned at a start position of the basic block (Figures 4, 6, & 7; column 12, lines 14-30). Wahbe does not teach an operation specifying unit for specifying an operation to be executed by the virtual machine.

47. Tremblay teaches an operation specifying unit for specifying an operation to be executed by the virtual machine (Figures 1 & 2; column 5, line 36 to column 6, line 54). It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the addressing of Tremblay with the system of Wahbe, because it would create a quicker and more efficient method to access the next sequence of data.

48. As per claim 44, Wahbe teaches the basic blocks (Figures 4, 6, & 7; column 11, line 58 to column 12, line 13); and,

49. identification tags, each designates an address related information of the virtual machine instruction at a start position of the basic block; attachment of the tag indicating if the virtual machine instruction corresponding to the identification tag is positioned at the start position of the basic block (Figures 4, 6, & 7; column 12, lines 14-30).

50. As per claims 49 through 51, Wahbe teaches a computer-readable recording medium for recording a program that enables a computer to carry out the storage method (Figures 1 through 3; column 5, line 20 to column 7, line 12).

***Conclusion***

51. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

52. The following patents are cited to further show the state of the art with respect to job scheduling, such as:

United States Patent No. 6,125,439 to Tremblay et al., which is cited to show a process of executing a method on a stack-based processor.

United States Patent No. 4,587,612 to Fisk et al., which is cited to show an accelerated instruction mapping external to source and target instruction streams for near real time injection into the latter.

United States Patent No. 5,428,754 to Baldwin, which is cited to show a computer system with a clock shared between the processors executing separate instruction streams.

United States Patent No. 5,748,806 to Gates, which is cited to show a Deskew circuit in a host interface circuit.

United States Patent No. 6,075,935 to Ussery et al., which is cited to show a method of generating application specific integrated circuits using a programmable hardware architecture.

United States Patent No. 5,933,104 to Kimura, which is cited to show a method for compression and decompression.

United States Patent No. 5,889,986 to Nguyen et al., which is cited to show and instruction fetch unit.

United States Patent No. 6,065,108 to Tremblay et al., which is cited to show an instruction identifier.

United States Patent No. 5,561,785 to Blandy et al., which is cited to show a system for allocating and returning storage and collecting garbage using a subpool of available blocks.

53. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian La Forgia whose telephone number is (703) 305-7704. The examiner can normally be reached on Monday thru Thursday 7-5.

54. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (703) 308-7562. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7240 for regular communications and (703) 746-7239 for After Final communications.

55. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JOHN A. FOLLANSBEE
PRIMARY EXAMINER

Christian La Forgia
Patent Examiner
Art Unit 2157

clf
October 8, 2002